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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,134	11/15/2001	Linden Minnick	042390P12310	6022

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EXAMINER	
TRUONG, LECHI	

ART UNIT	PAPER NUMBER
2194	

DATE MAILED: 11/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,134	MINNICK ET AL.	
	Examiner	Art Unit	
	LeChi Truong	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1,3-12,14-23,25-28 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-12, 14-23, 25-28, 30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-11, 12, 14-22, 23, 25-27, 28, and 30-34 are presented for examination. Claims 2, 13, 24, 29 are cancelled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5, 11, **12, 16, 17, 23, 28, 33, 34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) and further in view Fischer(US. Patent 4,783730).

3. As to claim 1, Harrington teaches the invention substantially as claimed including: a plurality of operation descriptors (corresponding blocks/list of command sequences, col 2, ln 15-20/ control block lists, col 18, ln 49-55), a controller (I/O controller, col 2, ln 15-20), issuing a plurality of commands to a controller, wherein the operational descriptors are issued in a first order (corresponding blocks or lists of command sequences, appropriate commands of each sequence are stored in the I/O controller local memory at any one time for suitable execution, col 2, ln 15-20/col 4, ln 18-22/ ln 42-46), each operating descriptor includes a command(col 18, ln 49-53), indicating the completion status of commands is indicated in a second order (Once a

complete sequence of commands from any control block list has been performed, the requester 15 provide return information to the host CPU notifying the latter the such sequence has been completed and proving suitable status information concerning the state, col 4, ln49-55), the term the second order is capable of being different from the first order (the commands are issued to the controller for execution at the same time[first order], col 2, ln 15-20/col 4, ln 18-22/ ln 42-46, . After completed the execution of all the commands, the indication for the completion of commands is provided [the second order], col 4, ln49-55).

4. Harrington do not explicitly teach include the operating descriptors includes a memory address identifying a memory location to which the completion status will be written, a value to be written upon completion of the command. However, Fischer teaches include a memory address identifying a memory location to which the completion status will be written, a value to be written upon completion of the command (the recipient of the Command/ status Doubleword 50[operational descriptor], col 9, ln 10-11/In the Command/Status Doubleword 50a as shown in Fig.9, the command byte is at bits 0 to 7 and is used to hold the command code... Bits 27 to 24 [address] hold the command completion status which in the case of a Mailbox indicate an operation completed successfully [completion status of the command], col 13, ln 18-20 and ln 27-30 / a done status can be indicated by the two status flags at bit 30 and 31. A done status indicates that processing of the command specified by this control structure has been completed, col 11, ln 5-9/ "01" for done [value to written upon completion], col 11, ln 15-17).

5. It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington and Fischer because Fischer's include a command, a memory address identifying a memory location to which the completion status will

be written, a value to be written upon completion of the command would improve the efficiency of Harrington's system by allowing the throughput of the system is improved by utilizing the indication status in the command status.

6. **As to claim 5**, Fischer teaches each command is stored in a first memory location, the complete status is written to a second memory location different form the first memory location (the command /status Doubleword 50 is a 32 bit entity that is divided into two 15 bit words. The high order word bits 16-31 contain status information. The low order word bits 0 to 15 include command information, col 8, ln 65-68 to col 9, ln 1-5/ the recipient thereafter perform the command and reports the successful completion of the command or an error condition upon attempting to execute that command. This reporting on the status of the command is written into the higher order word of the Command/ Status Doubleword, col 9, and ln 14-20).

7. **As to claim 11**, Harrington teaches the value to be written indicated the command's original location (col 11, ln 60-65).

8. **As to claim 12**, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above. In additional, Harrington teaches a machine –readable medium having instruction (col 3, ln 10-15).

9. **As to claims 16, 17,** they are apparatus claims of claims 11, 5; therefore, they are rejected for the same reasons as claims 11, 5 above.

10. **As to claim 23**, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above.

11. **As to claim 28**, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above. In additional, Harrington teaches a plurality of computation units (col 4, ln 6-9).

12. **As to claim 33**, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim above. In additional, Harrington teaches executing the commands in a first order (corresponding blocks or lists of command sequences, appropriate commands of each sequence are stored in the I/O controller local memory at any one time for suitable execution, col 2, ln 15-20/ the host execute the commands in an established sequence, col 4, ln 4, ln 42-44/ Once a complete sequence of commands from any control bocks has been performed [first order], the register 15 provide return information for the host CPU notifying the latter that such sequence has been completed[second order], col 4, ln 49-55).

13. **As to claim 34,** it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above.

14. Claims **3, 4, 14, 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) in view of Fischer (US. Patent 4,783730) and further in view of Kohn (US. Patent 4,366,536).

15. As to claims 3, 4, Harrington and Fischer do not teach an absolute address and an offset from a base memory address. However, Kohn teaches an absolute address and an offset from a base memory address (address indicated the offset, the absolute variable data are addresses, col 2, ln 8-16/ ln 42-45).

16. It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington, Fischer and Kohn because Kohn's address indicated the offset, the absolute variable data are addresses would improve the efficiency of Harrington and Fischer's systems by providing addresses to the respective memories and the program counter to the respective memories to make the i/o system more consistent.

17. As to claims 14, 15, they are apparatus claims of claims 3, 4; therefore, they are rejected for the same reasons as claims 3, 4 above.

18. Claims **6-9, 18-21, 25-26, 30-31** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) in view of Fischer (US. Patent 4,783730), as applied to claim 1 above, and further in view of Saito (US. Patent 6,567,862 B1).

19. As to claim 6, Harrington and Fischer do not teach the commands are grouped into categories. However, Saito teaches the commands are grouped into categories (groups received commands and stored commends to predetermined command group are according to group, col 2, ln 28-35).

20. It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington, Fischer and Saito because Saito's groups received commands and stored commends to predetermined command group are according to group would improve the flexibility of Harrington, Fischer 's systems by allowing movement of a recording head of the data server to be reduced. Therefore, the efficiency of disk access could be improved.

21. **As to claims 7, 8, 9**, Saito teaches their execution time/ a plurality of resource executes / a plurality of memory location (according to a recording area on the data recording medium accessed by each command, col 3, ln 1-5/based on this address information... corresponding to the access disk, col 8, ln 45-56/ at the command execution time T', col 12, ln 41-42).

22. **As to claims 18-21, 25-26, 30-31**, they are apparatus claims of claims 6-9; therefore, they are rejected for the same reasons as claims 6-9 above.

23. Claims **10, 22, 27, 32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) in view of Fischer (US. Patent 4,783730), as applied to claim 1 above, in view of Saito (US. Patent 6,567,862 B1) and further in view of Ghaffari et al (US. Patent 6,088,740).

24. **As to claim 10**, Harrington, Fischer and Saito do not teaches a single memory location. However, Ghaffari teaches a single memory location (a set of n command blocks 210-211, col 4, ln 4-10).

25. I would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington, Fischer, Saito and Ghaffari because Ghaffari's a single memory location improve the reliability of Harrington, Fischer, Saito 's systems by executing discrete commands quickly and efficiently for an error recovery when necessary.

26. **As to claims 22,27, 32**, they are apparatus claims of claim 10; therefore, they are rejected for the same reason as claim 10 above.

Response to the argument

27. Applicant's arguments filed 09/06/2006 have been considered but are moot in view of the new ground(s) of rejection. Applicant amended the claims. Harrington and Fischer references meet the amended claims.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LeChi Truong whose telephone number is (571) 272 3767. The examiner can normally be reached on 8 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomson, William can be reached on (571) 272 3718. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR of Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

LeChi Truong

November 21, 2006

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